COMPUTER-AIDED DESIGN FOR THE 1980's

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ABSTRACT

This paper describes a new, third generation computer program called SUPER-COMPACT, that opens a new era in automated microwave circuit design. Although the program is moderately large (approximately 50,000 FORTRAN statements), it can be run efficiently on midi-computers, as well as on most of the large-scale computer systems. The program combines analysis, optimization, and synthesis with interactive graphics for maximum user convenience and efficiency. Databanks, which provide scattering and noise parameters for transistors, dielectric information for substrate materials, and a library of available circuit topologies are integral to the program. While SUPER-COMPACT retains all of the previous capabilities of its first and second generation predecessors,[1,2,3] it uses a completely new approach to analyze and optimize microwave circuits. The program utilizes a novel interconnection scheme based upon scattering parameters without requiring the manipulation of large matrices. Both the inputting and outputting of data are handled through interactive graphic terminals.

Program Description

SUPER-COMPACT was created as the outcome of nearly ten years of experimentation to provide a single, general-purpose program to fulfill most needs of a microwave circuit designer. Several years of research, including a survey of about 5,000 designers, was spent to determine the input/output format and list of capabilities that satisfy the needs of the experts but be simple enough to be used by beginners. The result is a combination of numerous programs and subprograms to provide convenient data file creation and editing, circuit analysis and optimization, matching network synthesis, coupler and transmission line analysis, as well as several large databanks containing vital information on transistors and dielectric substrate materials.

Some of the capabilities of the program will be illustrated through the design of a 2-4 GHz low-noise amplifier. Specifications include 10 ±1 dB gain and noise figure less than 2 dB within the octave passband. The design procedure is the following;

Selection of the Active Device

The transistor should have optimum noise figure (NF_{opt}) of less than 1.8 dB (allowing .2 dB for input circuit losses) with associated gain in excess of 10 dB between 2-4 GHz. These specifications are submitted to the Transistor Databank[4] resulting in a list of devices, both FET and bipolar, that are capable of providing the desired gain. Any parameter of a specific transistor, including stability information, can be examined in either tabulated or graphical form. After a review of the available devices, a Hewlett-Packard HFET-1101 GaAs field-effect transistor was selected.

Device Modeling

The program models the input and output impedances of the transistor using the negative image device modeling[5] technique which provides the actual impedances presented by the device input and output under the desired gain and noise figure conditions. The modeling was done in terms of distributed elements since both input and output networks will be synthesized in distributed form. Lumped element modeling of the transistor input and output impedances could have been used if lumped-element matching had been desired. The resultant model is shown in Figure 1.

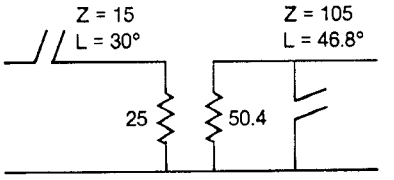

FIGURE 1: Transistor Equivalent Circuit

Topology Selection

Using the internally derived transistor impedance models, the program provides a list of alternative circuit topologies which may be synthesized for the given task. The user chooses a set of acceptable matching circuits by specifying the number of high-pass, low-pass and unit elements.

Matching Network Synthesis

The selected topology is submitted internally for synthesis; the program automatically selects the desired gain slope compensation by examining the transistor's gain versus frequency characteristic. The input equivalent circuit of the device includes a parasitic series open stub that presents problems to physical realization if not fully absorbed in the synthesis. The SUPER-COMPACT synthesis typically begins from the termination where the parasitic exists, and in this case the gain and ripple specifications are interactively adjusted until an "exact absorption" is reached -- meaning that the series stub will not have to be realized in the circuit.

Combining Data Files

At the completion of the synthesis, both networks are stored automatically in forms of disk files. Through the internal program editor, the user next combines the synthesized networks with the actual transistor. The synthesized circuit is shown on Figure 2.

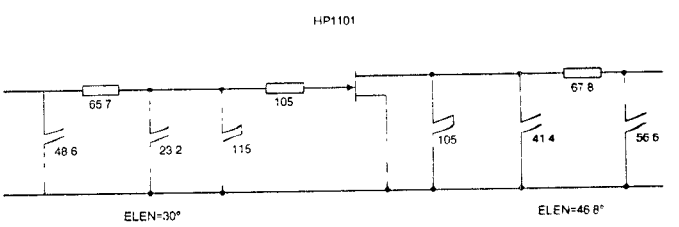

FIGURE 2: Initial Amplifier Circuit

149-645X/81/0000-0051$00.75

Initial Analysis and Optimization

The overall circuit is then analyzed and submitted for optimization. Due to the accurate device modeling, the synthesized circuit provides an excellent starting point for the optimization -- the initial gain variation was less than 1.5 dB. SUPER-COMPACT includes two different techniques: adaptive random and a gradient type. The combination of the two techniques assures a high degree of confidence in finding the global optimum of the circuit. In order to examine the interim performance, the optimization may be halted interactively at any time. The targeted gain of 10 dB was achieved with an overall flatness of ± 0.20 dB. The optimized response is shown in Figure 3.

Statistical Analysis

At the conclusion of the optimization, the circuit is submitted for a Monte Carlo analysis to examine the effects of active and passive component tolerances. Subsequent yield analysis shows the expected distribution of an actual production run, as shown on Figure 4.

Conversion to Physical Dimensions

Finally, the program offers a transmission line synthesis to convert the electrical parameters of the microstrip lines to physical dimensions. The microstrip models include the effects of dispersion, discontinuities, dielectric and conductor losses, and finite conductor thickness with multiple metallizations.[6] Although layout is not offered at this time, a future update to the program will also include the artwork generation.

Circuit: STAGE
S-matrix, ZS = 50. +j 0. ZL = 50. +j 0.

	S11		S21		S12		S22		|S21|
FREQ(Hz)	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
2.000E+09	0.930	-74.1	3.134	117.6	0.065	43.9	0.823	-19.6	9.922
2.500E+09	0.831	171.9	3.231	37.6	0.083	-31.6	0.695	-67.0	10.186
3.000E+09	0.762	89.5	3.098	-25.5	0.092	-90.2	0.616	-111.5	9.821
3.500E+09	0.652	3.6	3.186	-89.7	0.105	-149.7	0.532	-161.4	10.064
4.000E+09	0.536	-127.0	3.169	-169.9	0.113	135.0	0.411	132.8	10.019

NOISE FIGURE DATA

FREQ.	MIN. NOISE FIG.	OPT. NOISE SOURCE		ACTUAL NF	NORM
HZ	DB	MAGN	ANG	DB	RN
2.000E+09	1.25	0.352	86.8	1.39	0.104
2.500E+09	1.33	0.384	-164.6	1.54	0.047
3.000E+09	1.42	0.380	-90.6	1.69	0.174
3.500E+09	1.51	0.280	-9.3	1.69	0.311
4.000E+09	1.60	0.212	150.3	1.73	0.166

FIGURE 3: Optimized Data for the 2-4 GHz Amplifier

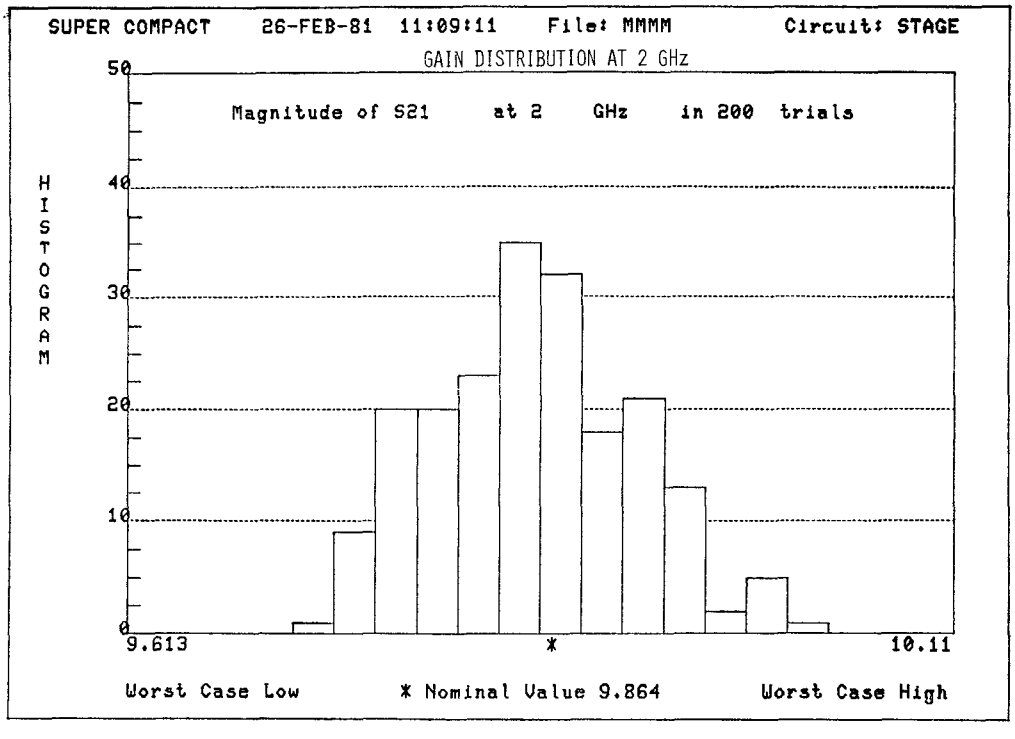

FIGURE 4: Histogram for 2 GHz Gain Distribution

Circuit Layout

At this point the design is completed. The final circuit with physical transmission line dimensions is shown in Figure 5. The corresponding wide band gain response is shown in Figure 6.

The 1980's will see computer-aided design of microwave circuits combined with automated layout and artwork generation, manufacturing, and test. SUPER-COMPACT will be expanded to offer interactive layout where the effects of significant parasitics and discontinuities will be accounted for during analysis and optimization.

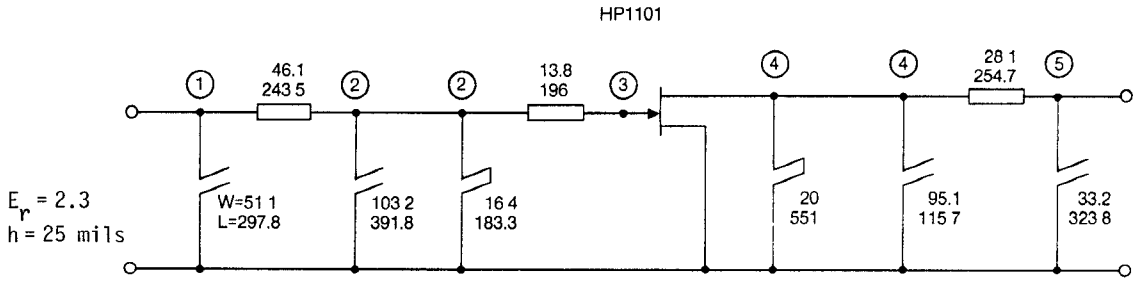

FIGURE 5: Optimized Circuit for 2-4 GHz Amplifier

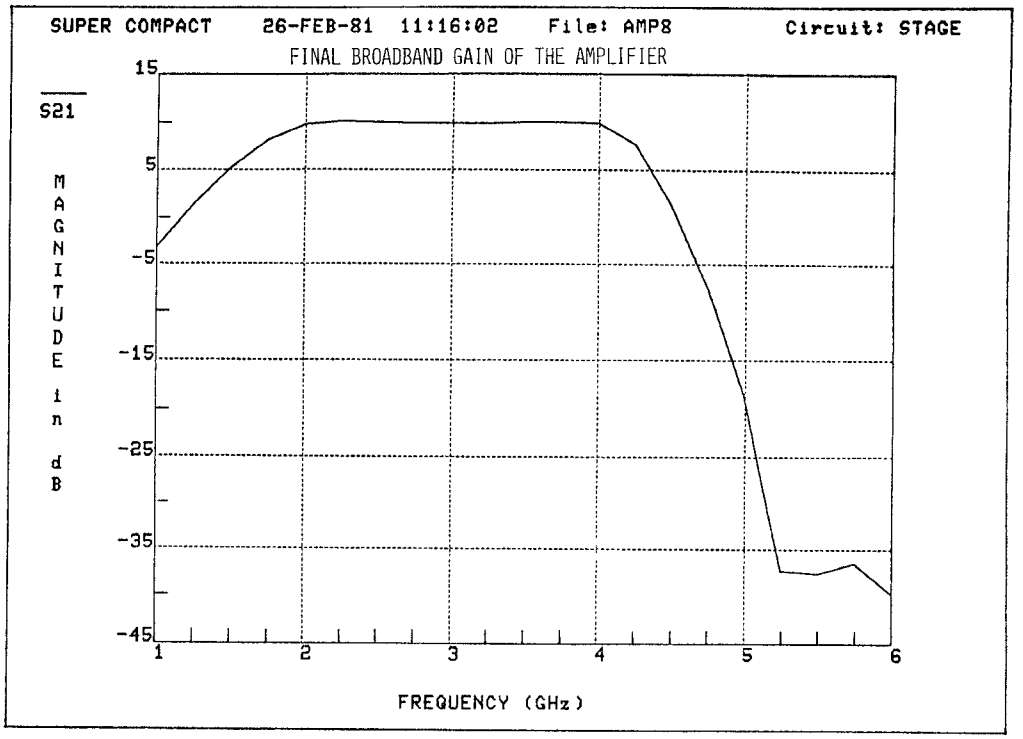

FIGURE 6: Broadband Gain for 2-4 GHz Amplifier

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